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Developing New 2D Materials and Heterostructures for Printed Digital Devices

2D-PRINTABLE - Deliverable report

D6.4 – Nanosheet-based memory devices

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Project Scientific Abstract

The 2D-PRINTABLE project aims to integrate sustainable large-scale liquid exfoliation techniques with theoretical modelling to efficiently produce a wide range of new 2D materials (2DMs), including conducting, semiconducting, and insulating nanosheets. The focus includes developing the printing and liquid phase deposition methods required to fabricate networks and multicomponent heterostructures, featuring layer-by-layer assembly of nanometer-thick 2DMs into ordered multilayers. The goal is to optimize these printed networks and heterostructures for digital systems, unlocking new properties and functionalities. The project also seeks to demonstrate various printed digital devices, including proof-of-principle, first-time demonstration of all-printed, all-nanosheet, heterostack light-emitting diodes (LEDs). In conclusion, 2D-PRINTABLE will prove 2D materials to be an indispensable material class in the field of printed electronics, capable of producing far-beyond-state-of-the-art devices that can act as a platform for the next generation of printed digital applications.

Public summary

The main objective of the deliverable D6.4 is to demonstrate high-performance ferroelectric memory. Devices using a hybrid gate dielectric composed of P(VDF-TrFE) polymer and CIPS ferroelectric nanosheets have been employed. The incorporation of CIPS nanosheets enhanced dipole alignment and improved the ferroelectric properties of the dielectric layer, leading to better memory performance in MoS_2 ferroelectric transistors. The optimized devices showed enhanced carrier transport, stable nonvolatile switching, reliable retention beyond 10,000 s, and endurance over 300 switching cycles. The study highlights the potential of hybrid polymer/2D ferroelectric systems for scalable, low-power, and high-performance nonvolatile memory applications.

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Abbreviations & Definitions

Abbreviation	Explanation
2D	Two-dimensional
MoS_2	Molybdenum disulfide
vdW	van der Waals
CIPS	$CuInP_2S_6$
P(VDF-TrFE)	poly(vinylidene fluoride–trifluoroethylene)
MEK	methyl ethyl ketone

1 Introduction

Solution-processable two-dimensional (2D) material inks have recently emerged as promising building blocks for next-generation printed electronics owing to their compatibility with scalable, low-temperature, and large-area fabrication techniques. In particular, liquid-phase exfoliated 2D nanosheets can be formulated into printable inks that enable the deposition of functional electronic layers through solution-based processes, offering an attractive alternative to conventional vacuum-based fabrication methods.

Among emerging printable 2D materials, layered van der Waals (vdW) ferroelectrics such as $CuInP_2S_6$ (CIPS) are especially attractive for nonvolatile memory applications because they combine atomically thin geometry with switchable out-of-plane polarization. Importantly, CIPS can be exfoliated into stable liquid dispersions, enabling the development of printable ferroelectric nanosheet inks suitable for scalable electronic and optoelectronic device fabrication.

Despite these advantages, the direct integration of 2D ferroelectric inks into reliable memory devices remains challenging due to difficulties associated with film uniformity, polarization stability, and large-area device integration. To address these limitations, hybrid ferroelectric systems combining printable 2D ferroelectric inks with conventional ferroelectric polymers provide a promising strategy. In particular, poly(vinylidene fluoride–trifluoroethylene) [P(VDF-TrFE)] offers excellent solution processability, mechanical flexibility, and well-established ferroelectric switching behavior, making it an ideal matrix for embedding functional 2D ferroelectric nanosheets.

In this work, we developed a novel printable hybrid ferroelectric platform by incorporating liquid-phase exfoliated CIPS nanosheet inks into a P(VDF-TrFE) matrix. The resulting nanosheet-embedded hybrid system enables cooperative ferroelectric coupling between the 2D nanosheets and the polymer dipoles, leading to reinforced polarization behavior and improved dielectric functionality. The hybrid ferroelectric inks were subsequently employed as gate dielectric layers in molybdenum disulfide (MoS_2)-based ferroelectric memory transistors fabricated through solution-compatible processes.

2 Methods and core part of the report

2.1 Background

P(VDF-TrFE) is one of the most widely used solution-processable ferroelectric polymers for nonvolatile memory applications due to its stable polarization switching and excellent film-forming characteristics. However, further enhancement of polarization strength and charge-storage capability is desirable for high-performance memory devices.
CIPS is a layered vdW ferroelectric material that can be exfoliated into nanosheets and processed as printable inks. The incorporation of ferroelectric nanosheets into a polymer matrix provides a potential route to reinforce polarization behavior through cooperative ferroelectric interactions.
Therefore, hybrid P(VDF-TrFE)/CIPS ferroelectric inks were utilized as gate dielectric materials in MoS_2 memory transistors, and their effects on memory storage, retention and endurance functionality were systematically evaluated.

2.2 Procedures

2.2.1 Preparation of P(VDF-TrFE)/CIPS Hybrid Films

CIPS nanosheets were prepared by liquid-phase exfoliation in isopropanol (IPA). P(VDF-TrFE) was dissolved in methyl ethyl ketone (MEK), and the CIPS dispersion was subsequently mixed with the polymer solution to produce hybrid ferroelectric inks with different CIPS concentrations. The resulting solutions were spin-coated onto substrates and thermally annealed at 142 °C on a hot plate for 2 h in N_2 to crystallize the ferroelectric polymer phase.

2.2.2 Fabrication of MoS_2 Ferroelectric Memory Transistors

Bottom-gate ferroelectric transistors were fabricated on SiO_2/n^+-Si substrates. Au/Cr bottom gate electrodes were patterned by photolithography and thermal evaporation. Hybrid P(VDF-TrFE)/CIPS films were spin-coated as ferroelectric gate dielectrics. Multilayer MoS_2 flakes were transferred onto the dielectric layer using a PDMS-assisted transfer method. Finally, Au source/drain electrodes were deposited using the same methods as for the bottom electrode.

2.2.3 Characterization

Ferroelectric properties of the hybrid films were evaluated using polarization–electric field (P–E) and capacitance–voltage (C–V) measurements. Structural characterization was performed using X-ray diffraction (XRD), Raman spectroscopy, and atomic force microscopy (AFM). Electrical characterization of the memory transistors was carried out using semiconductor parameter analyzers under ambient conditions. Retention and endurance measurements were conducted by applying positive and negative gate-voltage pulses corresponding to Program and Erase states.

2.3 Data Analysis

OriginLab software was used to carry out data analysis.

3 Results & Discussion

3.1 Results

3.1.1 Enhanced Ferroelectricity in P(VDF-TrFE)/CIPS Hybrid Films

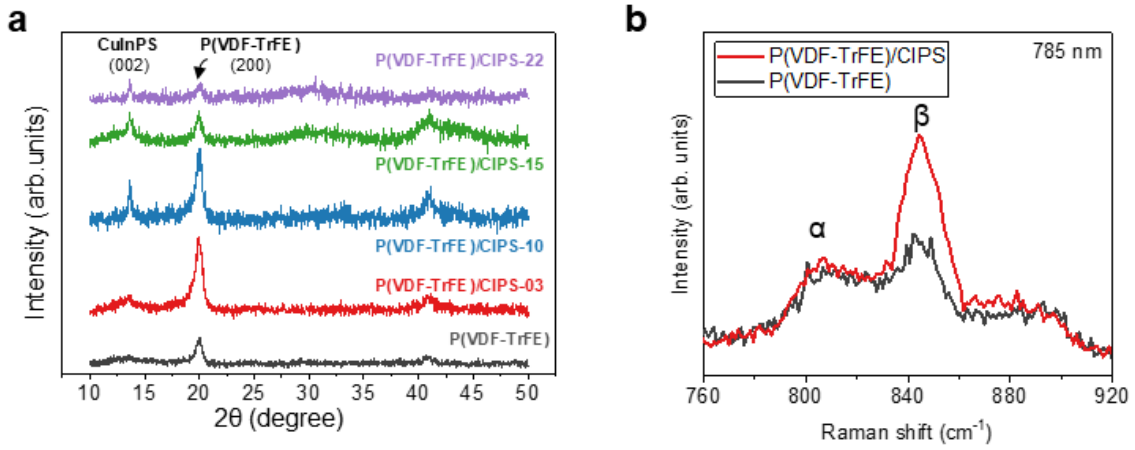

Figure 1. P(VDF-TrFE)/CIPS characterization. a) XRD patterns of pristine P(VDF-TrFE) and P(VDF-TrFE)/CIPS hybrid films with varying CIPS contents. b) Raman spectra of pristine P(VDF-TrFE) and P(VDF-TrFE)/CIPS-03 films under 785 nm laser excitation.

The incorporation of ultrathin CIPS nanosheets into the P(VDF-TrFE) matrix significantly enhanced the ferroelectric properties of the polymer film. As shown in Figure 1, XRD and Raman analyses revealed enhanced ferroelectric β-phase formation in the hybrid films compared with pristine P(VDF-TrFE), indicating improved dipole ordering induced by the ferroelectric CIPS nanosheets. To systematically examine the effect of CIPS incorporation, the hybrid solutions were labelled P(VDF-TrFE)/CIPS-03, -10, -15, and -22, corresponding to final (i.e. post-mixing) CIPS concentrations of 0.03, 0.10, 0.15, and 0.22 mg mL^{-1}, respectively.

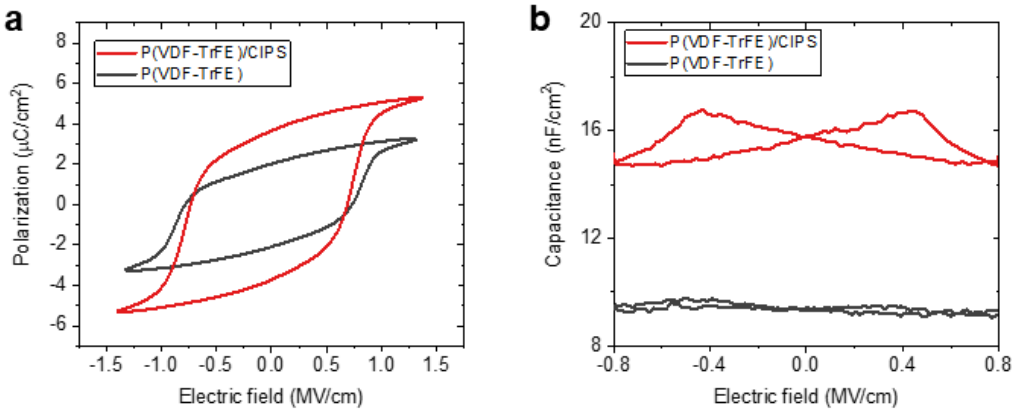

Figure 2. Electrical characterization. a) P-E hysteresis loops of Au/P(VDF-TrFE)/Au and Au/P(VDF-TrFE)/CIPS/Au capacitors on SiO_2 substrates, measured at 100 Hz. b) C-V characteristics of the same capacitor structures measured at 1 kHz.

Electrical characterization further confirmed the cooperative ferroelectric behavior (Figure 2). The remnant polarization (P_r) increased from approximately 2.02 µC cm^{-2} for pristine P(VDF-TrFE) to 3.67 µC cm^{-2} for the optimized P(VDF-TrFE)/CIPS-03 hybrid film, corresponding to an enhancement of nearly 75%. Simultaneously, the coercive field decreased from approximately 0.75 MV cm^{-1} to 0.69 MV cm^{-1}, indicating facilitated polarization switching. In addition, the capacitance of the hybrid dielectric increased from approximately 9 nF cm^{-2} to 16 nF cm^{-2}, reflecting enhanced dielectric polarization and charge-storage capability of the hybrid dielectric layer.

3.1.2 Quantification of Memory Storage Capability

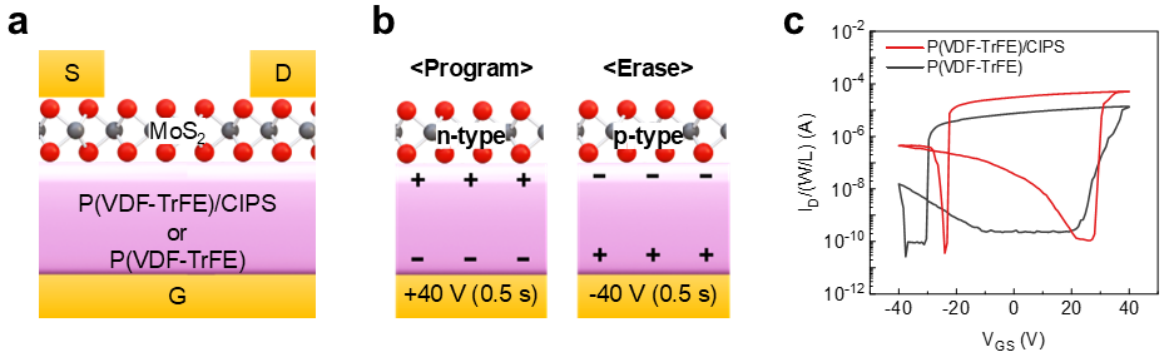

Figure 3. **Ferroelectric memory transistor.** a) 2D illustration of the MoS_2-based ferroelectric memory transistor. b) Schematics depicting two nonvolatile polarization states in the device: Program (electron-accumulation) state and Erase (hole-accumulation) state. c) Transfer characteristics of the MoS_2-based ferroelectric memory transistor.

As depicted in Figure 3c, compared with control devices using pristine P(VDF-TrFE), the hybrid dielectric enabled substantially stronger carrier modulation. At positive gate voltages, the drain current increased by approximately 3.4 times, indicating enhanced electron accumulation. Under negative gate voltages, the hole current increased by more than one order of magnitude, demonstrating efficient hole accumulation in the MoS_2 channel. Interestingly, the hybrid devices also exhibited substantially enhanced memory-state currents at V_{GS} = 0 V, directly reflecting their improved charge-storage capability. The Program-state current increased from approximately 7.5 µA to 30 µA, while the Erase-state current increased from 0.24 nA to 36 nA compared with pristine P(VDF-TrFE)-based devices. In addition, the devices exhibited stable hysteretic transfer characteristics associated with nonvolatile ferroelectric switching. The reduced coercive field of the hybrid dielectric contributed to lower switching voltages while maintaining stable memory operation.

3.1.3 Retention and Endurance Characteristics

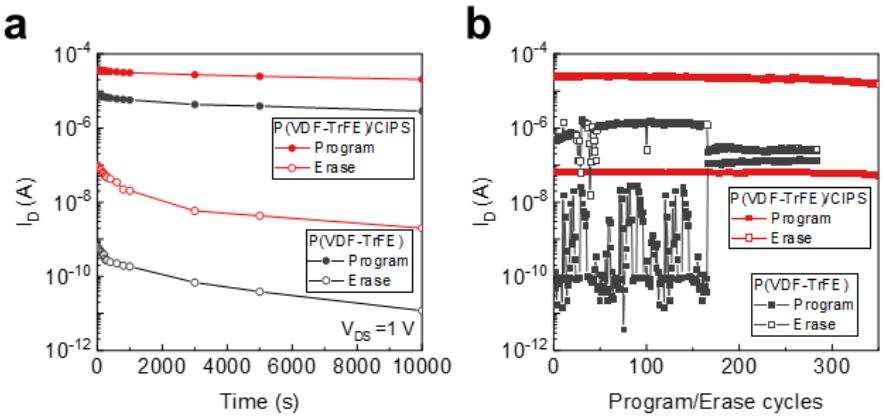

Figure 4. **Retention and endurance characteristics.** a) Retention properties, and f) cyclic endurance results of MoS_2/P(VDF-TrFE)/CIPS FET (red) and MoS_2/P(VDF-TrFE) FET (black) measured at V_{DS} = 1 V.

The retention behavior of the memory transistors was investigated by monitoring the drain current after applying Program and Erase voltage pulses (Figure 4a and b). Both memory states remained stable for more than 10,000 s, demonstrating reliable long-term nonvolatile operation (Figure 4a). Endurance measurements further highlighted the improved operational stability enabled by the hybrid dielectric (Figure 4b). Devices based on pristine P(VDF-TrFE) exhibited significant current fluctuations and degradation after approximately 160 switching cycles. In contrast, MoS_2/P(VDF-TrFE)/CIPS devices maintained stable Program and Erase states for more than 300 switching cycles without significant degradation. These results confirm that the incorporation of ferroelectric CIPS nanosheets substantially improves memory retention stability and switching endurance in nanosheet-based ferroelectric memory devices.

3.2 Contribution to project (linked) Objectives

The demonstrator of this deliverable contributes extending the target of the objective O6.3 “Demonstration of integration of high-mobility TFTs into simple circuits” to memory devices.

3.3 Contribution to major project exploitable result

This demonstrator directly supports Task 6.6 “Non-volatile memories” by taking the first steps toward integrating TFTs based on 2D semiconductors in memory devices through the employment of ferroelectric copolymers.

4 Conclusion and Recommendation

In this work, nanosheet-based ferroelectric memory devices employing hybrid P(VDF-TrFE)/CIPS gate dielectrics were successfully demonstrated. The incorporation of ferroelectric CIPS nanosheets into the polymer matrix reinforced dipole ordering and substantially enhanced the ferroelectric properties of the dielectric layer. The improved ferroelectricity enabled enhanced memory storage capability in MoS_2 ferroelectric memory transistors, including stronger carrier accumulation, increased carrier mobility, stable nonvolatile switching, and improved retention and endurance characteristics. The optimized devices exhibited reliable retention beyond 10,000 s and stable operation over more than 300 switching cycles. Overall, the results demonstrate that hybrid ferroelectric systems combining polymer ferroelectrics with 2D ferroelectric nanosheets provide a promising strategy for scalable, low-power, and high-performance nonvolatile memory electronics.

5 Risks and interconnections

5.1 Risks/problems encountered

Risk No.	What is the risk	Probability of risk occurrence[1]	Effect of risk[1]	Solutions to overcome the risk
-	-	-	-	-

[1)] Probability risk will occur: 1 = high, 2 = medium, 3 = Low

5.2 Interconnections with other deliverables

Not applicable

6 Deviations from Annex 1

Not applicable

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Project partners:

#	Partner short name	Partner Full Name
1	TCD	TCD THE PROVOST, FELLOWS, FOUNDATION SCHOLARS & THE OTHER MEMBERS OF BOARD, OF THE COLLEGE OF THE HOLY & UNDIVIDED TRINITY OF QUEEN ELIZABETH NEAR DUBLIN
2	UNISTRA	UNIVERSITE DE STRASBOURG
3	UKa	UNIVERSITAET KASSEL
4	BED	BEDIMENSIONAL SPA
5	TUD	TECHNISCHE UNIVERSITAET DRESDEN
6	VSCHT	VYSOKA SKOLA CHEMICKO-TECHNOLOGICKA V PRAZE
7	UNR	UNIRESEARCH BV
8	UniBw M	UNIVERSITAET DER BUNDESWEHR MUENCHEN
9	EPFL	ECOLE POLYTECHNIQUE FEDERALE DE LAUSANNE

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