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Developing New 2D Materials and Heterostructures for Printed Digital Devices

2D-PRINTABLE - Deliverable report

D6.3. – Nanosheet-based inverters

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Project Scientific Abstract

The 2D-PRINTABLE project aims to integrate sustainable large-scale liquid exfoliation techniques with theoretical modelling to efficiently produce a wide range of new 2D materials (2DMs), including conducting, semiconducting, and insulating nanosheets. The focus includes developing the printing and liquid phase deposition methods required to fabricate networks and multicomponent heterostructures, featuring layer-by-layer assembly of nanometer-thick 2DMs into ordered multilayers. The goal is to optimize these printed networks and heterostructures for digital systems, unlocking new properties and functionalities. The project also seeks to demonstrate various printed digital devices, including proof-of-principle, first-time demonstration of all-printed, all-nanosheet, heterostack light-emitting diodes (LEDs). In conclusion, 2D-PRINTABLE will prove 2D materials to be an indispensable material class in the field of printed electronics, capable of producing far-beyond-state-of-the-art devices that can act as a platform for the next generation of printed digital applications.

Public summary

The main objective of the deliverable D6.3 is to provide a demonstrator consisting of logic inverters based on 2D semiconducting nanosheets that achieve reliable binary switching and high voltage gain. 2D-PRINTABLE partners successfully integrated sonication-exfoliated VP nanosheets and MoS_2 flakes as p-type and n-type channels, respectively, into functional devices. Uniform films and well-connected p–n transistor pairs were obtained to ensure efficient charge transport and stable device operation. The fabricated logic inverters exhibited clear “0” and “1” output states with a voltage gain >15, demonstrating the feasibility of low-power, printable 2D logic circuits.

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Abbreviations & Definitions

Abbreviation	Explanation
2D	Two-dimensional
MoS_2	Molybdenum disulfide
VP	Violet phosphorus
PS-PEO-PS	Polystyrene-poly(ethylene oxide)-polystyrene
DMF	Dymethilformamide
IPA	2-propanol
[EMIM][TFSI]	1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide
V_G	Gate voltage
V_{in}	Input voltage
V_{out}	Output voltage
V_{DD}	Supply voltage
GND	Ground

1 Introduction

The field of printed electronics is rapidly evolving, driven by solution-processed 2D semiconductors that enable low-power, flexible, and large-area electronic circuits. Among the key components of digital electronics, logic inverters play a central role in converting input signals into complementary output states, forming the foundation of more complex circuits. Printable 2D semiconductors such as violet phosphorus (VP) and molybdenum disulfide (MoS_2) are particularly promising for this application, providing complementary p-type and n-type behavior in a form compatible with solution processing. However, realizing functional logic inverters with 2D materials presents several challenges. Uniform film formation, sufficient nanosheet connectivity, low junction resistance, and reproducible deposition are critical to ensure reliable switching, well-defined binary output states, and adequate voltage gain. Additionally, variability in nanosheet size, thickness, and orientation can further affect device performance, making the fabrication of high-quality p–n transistor pairs a nontrivial task.

In this demonstrator, VP nanosheets and MoS_2 flakes were exfoliated using sonication-assisted methods to produce stable inks, which were deposited to form p–n transistor pairs for logic inverters. The devices successfully achieved clear “0” and “1” output states and high voltage gain, confirming that the essential requirements for printed 2D logic inverters were met and directly supporting Task 6.5 “Inverters.”

These results demonstrate the feasibility of integrating complementary 2D semiconductors into scalable, low-power printed logic circuits.

2 Methods and core part of the report

2.1 Background

Inks of 2D materials were prepared via sonication-assisted exfoliation of bulk VP and MoS_2 crystals. These inks were used to fabricate uniform films and networks suitable for device integration. Finally, the resulting films were incorporated into logic inverters, and their input-output characteristics and voltage gain were evaluated to benchmark device performance.

2.2 Procedures

Bulk VP crystals were first synthesized by a chemical vapor transport method using a mixture of red phosphorus, tin, and tin(IV) iodide sealed under vacuum and subjected to a controlled multi-step heating protocol to promote nucleation and minimize clustered black phosphorus formation. For liquid-phase exfoliation, the VP crystals were ground with a mortar and pestle and dispersed in degassed anhydrous solvents (ethanol, 2-propanol (IPA), dimethylformamide (DMF), acetone) and water at 1 mg mL^{-1}. The dispersions were sonicated for 5 hours at 65% amplitude (6 s on, 2 s off) using a QSonica Q700 sonicator while keeping the samples cooled, and DMF was selected for further studies due to its superior stability after 48 hours. Similarly, MoS_2 was exfoliated in N-methyl-2-pyrrolidone (NMP) following the same procedure, yielding stable few-layer dispersions after centrifugation to remove unexfoliated material. For device fabrication, logic inverter structures were patterned on substrates using AZ1505 photoresist with MIF726 developer via laser photolithography. Source and drain electrodes were defined by thermally evaporating 5 nm chromium and 40 nm gold, followed by lift-off and rinsing with acetone and 2-propanol. Exfoliated VP from DMF and MoS_2 from IPA was drop-cast onto the substrates and annealed at 200 °C for 2 hours under nitrogen. A triblock copolymer ion gel composed of PS-PEO-PS blended with [EMIM][TFSI] and dissolved in acetonitrile was subsequently drop-cast onto the dried VP films. Electrical characterization of the devices was carried out under nitrogen using a Keithley 2636A source meter for logic inverter measurements.

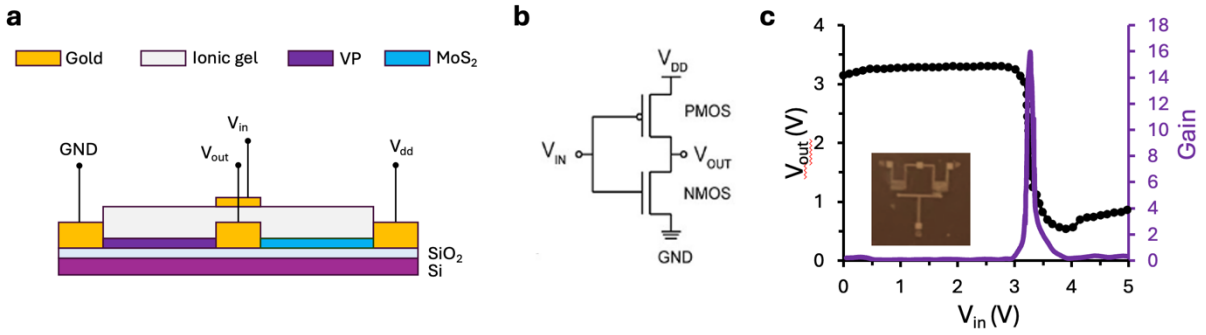
2.3 Data Analysis

OriginLab software was used to carry out data analysis.

3 Results & Discussion

3.1 Results

A logic inverter was fabricated using VP nanosheets as the p-type (PMOS) channel material and MoS_2 flakes as the n-type (NMOS) channel. The VP and MoS_2 flakes were drop-cast onto the substrate to form the respective transistors. The device layout and optical image are presented in Figure 1. The channel length of the interdigitated electrodes were ranged between 10 and 20 µm, in order to find the optimized conditions. When the input voltage is swept from 0 to 5 V (V_{DD} = 3 V), the inverter exhibits clear binary output states ("1" and "0"), with a sharp transition corresponding to a voltage gain of approximately >15. This performance is comparable to leading HfO_2-gated 2D logic inverters



based on liquid-phase exfoliated materials,[1] highlighting the suitability of our solution-processed device for low-power 2D logic systems.

Figure 1. Logic inverter architecture and device output. (a) Schematic illustration of the inverter. Ground (GND), input voltage (V_{in}), output voltage (V_{out}). (b) Schematic illustration of the electrical circuit of the demonstrator. (c) V_{in} – V_{out} characteristics (black) and voltage gain (purple) of the logic inverter.

3.2 Contribution to project (linked) Objectives

The demonstrator of this deliverable contributes reaching the target of the objective O6.3 "Demonstration of integration of high-mobility TFTs into simple circuits".

3.3 Contribution to major project exploitable result

This demonstrator directly supports Task 6.5 "Inverters" by taking the first steps toward integrating high-mobility printed p–n transistor pairs. Input-output characteristics and voltage gain were measured to evaluate the inverter performance.

4 Conclusion and Recommendation

This deliverable reports the fabrication and demonstration of a logic inverter using VP and MoS_2 films as the PMOS and the NMOS channels, respectively. The device exhibited clear binary output states and a high voltage gain >15, directly supporting Task 6.5 of WP6. These results demonstrate the feasibility of integrating printable p–n transistor pairs for 2D logic circuits. Future work will extend this approach to other 2D semiconductors, alternative deposition techniques, and larger-area devices to further advance low-power printed logic demonstrators.

5 Risks and interconnections

5.1 Risks/problems encountered

No risks incurred

5.2 Interconnections with other deliverables

Interconnections occur with D6.1 as channel materials used in inverters can be characterized separately in distinct TFTs.

6 Deviations from Annex 1

Not applicable

7 References

[1] Lin, Z.; Liu, Y.; Halim, U.; Ding, M.; Liu, Y.; Wang, Y.; Jia, C.; Chen, P.; Duan, X.; Wang, C.; Song, F.; Li, M.; Wan, C.; Huang, Y.; Duan, X. Solution-Processable 2D Semiconductors for High-Performance Large-Area Electronics. Nature 2018, 562, 254−258.

8 Acknowledgement

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Project partners:

#	Partner short name	Partner Full Name
1	TCD	TCD THE PROVOST, FELLOWS, FOUNDATION SCHOLARS & THE OTHER MEMBERS OF BOARD, OF THE COLLEGE OF THE HOLY & UNDIVIDED TRINITY OF QUEEN ELIZABETH NEAR DUBLIN
2	UNISTRA	UNIVERSITE DE STRASBOURG
3	UKa	UNIVERSITAET KASSEL
4	BED	BEDIMENSIONAL SPA
5	TUD	TECHNISCHE UNIVERSITAET DRESDEN
6	VSCHT	VYSOKA SKOLA CHEMICKO-TECHNOLOGICKA V PRAZE
7	UNR	UNIRESEARCH BV
8	UniBw M	UNIVERSITAET DER BUNDESWEHR MUENCHEN
9	EPFL	ECOLE POLYTECHNIQUE FEDERALE DE LAUSANNE

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9 Appendix A - Quality Assurance Review Form

The following questions should be answered by all reviewers (WP Leader, reviewer, Project Coordinator) as part of the Quality Assurance procedure. Questions answered with NO should be motivated. The deliverable author will update the draft based on the comments. When all reviewers have answered all questions with YES, only then can the Deliverable be submitted to the EC.

NOTE: This Quality Assurance form will be removed from Deliverables with dissemination level "Public" before publication.

Question	**WP Leader**	**Reviewer**	**Project Coordinator**
	P. Samorì (UNISTRA)	Georg Duesberg (UniBw M)	Jonathan Coleman (TCD)
1. *Do you accept this Deliverable as it is?*	Yes	Yes	Yes
2. *Is the Deliverable complete?* - *All required chapters?* - *Use of relevant templates?*	Yes	Yes	Yes
3. *Does the Deliverable correspond to the DoA?* - *All relevant actions preformed and reported?*	Yes	Yes	Yes
4. *Is the Deliverable in line with the 2D-PRINTABLE objectives?* - *WP objectives* - *Task Objectives*	Yes	Yes	Yes
5. *Is the technical quality sufficient?* - *Inputs and assumptions correct/clear?* - *Data, calculations, and motivations correct/clear?* - *Outputs and conclusions correct/clear?*	Yes	Yes	Yes
6. *Is created and potential IP identified and are protection measures in place?*	No potential IP was identified by partners	No potential IP was identified by partners	No potential IP was identified by partners
7. *Is the Risk Procedure followed and reported?*	Yes	Yes	Yes
8. *Is the reporting quality sufficient?* - *Clear language* - *Clear argumentation* - *Consistency* - *Structure*	Yes	Yes	Yes