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Developing New 2D Materials and Heterostructures for Printed Digital Devices

2D-PRINTABLE - Deliverable report

D3.3 – Printed heterostructure fabrication

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Project Scientific Abstract

The 2D-PRINTABLE project aims to integrate sustainable large-scale liquid exfoliation techniques with theoretical modelling to efficiently produce a wide range of new 2D materials (2DMs), including conducting, semiconducting, and insulating nanosheets. The focus includes developing the printing and liquid phase deposition methods required to fabricate networks and multicomponent heterostructures, featuring layer-by-layer assembly of nanometer-thick 2DMs into ordered multilayers. The goal is to optimize these printed networks and heterostructures for digital systems, unlocking new properties and functionalities. The project also seeks to demonstrate various printed digital devices, including proof-of-principle, first-time demonstration of all-printed, all-nanosheet, heterostack light-emitting diodes (LEDs). In conclusion, 2D-PRINTABLE will prove 2D materials to be an indispensable material class in the field of printed electronics, capable of producing far-beyond-state-of-the-art devices that can act as a platform for the next generation of printed digital applications.

Public summary

This report highlights advancements in fabricating vertical heterostacks using solution-processed 2D nanosheet networks. Compared to planar structures, vertical architectures enable significantly reduced channel lengths, lowering channel resistance and enhancing control over metal-semiconductor interfacial behaviours. However, achieving high-quality heterostacks at ultrathin active-layer thicknesses remains challenging due to pinhole defects in 2D networks and solvent-induced re-dispersion during multilayer deposition. We present optimized fabrication strategies, demonstrated through metal-insulator-metal (MIM) capacitors and metal-semiconductor-semiconductor-semiconductor-metal (MSSSM) LEDs.

We first introduce the fabrication of MIM structured capacitor. We took advantage of high aspect-ratio insulating perovskite nanosheets to form compact and pores-free nanosheet networks by dip coating. We used electrochemically exfoliated graphene and used spray coating to form metallic nanosheet networks on 2D networks. This graphene layer is of vital importance to avoid electrical shorts caused by the ultra-small pinholes on the 2D layer. This 2D top electrode strategy could be extended to other types of nanostructured thin films as well as device structures.

Next, we demonstrate the fabrication of MSSSM structured LEDs by spin coating. Electrochemically exfoliated MoS_2 nanosheets were used as the model material. Thickness of the MoS_2 thin film can be tuned simply by varying the coating cycles. To fabricate the device with a well-preserved interface quality, we proposed an orthogonal solvent selection for the functional materials from the bottom to the top layer, where the solvent re-dispersing issue can be greatly minimised. Furthermore, other types of nanomaterials or polymeric semiconductors such as poly-TPD or ZnO nanoparticles, can be utilised to form seamless network and block the pinholes on the 2D surface from metal diffusing.

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Abbreviations & Definitions

Abbreviation	Explanation
AFM	Atomic force microscopy
Poly-TPD	Poly(N,N'-bis-4-butylphenyl-N,N'-bisphenyl)benzidine
PEDOT:PSS	Poly(3,4-ethylenedioxythiophene) polystyrene sulfonate
CNNO	$Ca_2NaNb_3O_{10}$
DMF	Dimethylformamide

1 Introduction

This report deals with the progress made on Task 3.4 Fabrication of stacked heterostructures by printing, aiming at realising 2D materials based heterostructures by printing techniques.

Solution processed 2D materials based electronics are mostly relying on a lateral device structure where the device performance is largely limited by the high channel resistance. Reducing the channel resistance by decreasing the channel length is challenging to be achieved via solution-based techniques. A potential solution is to change to the vertically stacked device structure, where the channel length can be reduced from more than tens of micrometers to only tens of nanometers. Such a large reduction in the channel length will dramatically reduce the resistance in the channel, so the electrical behaviours at the metal/semiconductor interface could be developed and device performance can be improved.

Despite their advantages, vertical device structures face several key challenges. Pinhole formation remains a critical issue, which can be mitigated by increasing film thickness—however, this approach comes at the cost of higher channel resistance, ultimately degrading device performance. Additionally, interfacial re-dispersing during processing can further compromise the quality of the layered structure.

With the above identified fabrication problems, we propose our strategies to reliably fabricate the vertical heterostack such as capacitor and LEDs, regarding material and solvent selection, multi-layer deposition, and a combination of printing techniques. The tasks and objectives within this deliverable will be continued through the entire project. The techniques gained from this deliverable will be the foundation to fabricate various types of devices mentioned in other deliverables.

2 Methods and core part of the report

2.1 Background

In recent years, solution-processed 2D material-based electronic devices, particularly transistors, have emerged as a promising research area. Fundamental limitations have been found for laterally structured devices where the channel length, the spatial distance of two electrodes, is challenging to be further reduced with the current solution-processed techniques. The bulk resistance from the semiconductor channel is much larger than the contact resistance at the semiconductor/metal interfaces. Consequently, the electrical behaviour of the device is governed by the electrical properties of the bulk semiconductor. It is rare and difficult to observe any electrical behaviours coming from the semiconductor/metal interface (Schottky), which could lead to other applications, such as Schottky solar cells. To improve the electrical performance, it is desirable to reduce the channel length, i.e., the resistance from the channel. Further, once the bulk resistance is smaller or comparable to the contact resistance, the electrical behaviours coming from the interface can be explored and utilised to create novel devices.

A potential solution is transitioning to a vertically stacked device structure, where the channel length (determined by film thickness) can be reduced to tens of nanometers. This approach drastically lowers bulk resistance, enabling the development of interface-dominated electrical behaviours. However, vertical structures face challenges such as pinhole formation, which arises from factors like surface cleanliness, dispersion properties, nanomaterial morphology, and printing techniques. Pinholes can cause unintended direct contact between non-adjacent layers, leading to electrical shorts or current leakage. Additionally, re-dispersion of adjacent layers during solution processing can further degrade device performance.

In this deliverable, we will present our solution from material and solvent selection to the choice of printing techniques to overcome this issue and fabricate proof-of-concept devices such as capacitor and LEDs.

2.2 Procedures

Samples: MoS_2 was produced through our established electrochemical intercalation procedure. All solvents are HPLC grade and was purchased from Sigma-Aldrich. Poly(N,N'-bis-4-butylphenyl-N,N'-bisphenyl)benzidine (poly-TPD) and poly(3,4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS) were obtained from Ossila and was used as received. ZnO nanoparticle isopropanol dispersion was obtained from Sigma-Aldrich and was used as received.

Device fabrication: The ITO glasses (Ossila) were etched by diluted hydrochloric acid at 80 °C for 10 min. The etched ITO glasses were cleaned in Decon/DI water, DI water and isopropanol for 10 min in sequence by ultra-sonication in a sonic bath. The solvent-cleaned ITO glasses were further treated by O_2 plasma for 5 min by Diener PICO Barrel Asher. Dip coating was performed with a dip coater from Ossila. Spray coating was performed with a Harder and Steenbeck Infinity airbrush which was attached to a Janome JR2300N mobile gantry to spray the dispersion over a programmed area. The spraying process was done in ambient conditions. Spin coating was performed with a Laurell spin coater (WS-400A-8NPP/LITE).

Characterisations: UV-Vis spectroscopy was used to collect the transmission spectra of the poly-TPD thin film on glass and bare glass slide. The transmission spectra were converted into extinction spectra by Beer-Lambert Law. The poly-TPD extinction spectrum was obtained by subtracting the bare glass extinction spectrum. Atomic force microscopy was performed using a Bruker Multimode 8 microscope. Optical transmission scan was performed by Epson Perfection V700 photo flatbed scanner. The spatial resolution is 6400 dpi and spectral resolution is 48 bit. The point resolution of the image is about 4 μm.

2.3 Data Analysis

The AFM image was processed by Gwyddion. The optical scanned photo was processed by Image J. All numerical data was processed and analysed in Origin.

3 Results & Discussion

3.1 Results

In this section, we will demonstrate the methodology of choosing the morphologically and electronically suitable materials and printing techniques to realise vertical stacks.

3.1.1 Fabrication of vertically stacked MIM devices

Capacitor is a typical MIM type device where an insulator layer is sandwiched by two metal layers. Although the device structure is relatively simple, it is challenging to fabricate MIM with a thin insulating layer due to the presence of pinholes may result in a contact between top and bottom electrode, i.e., electrical shorts.[1] To overcome this issue, materials and printing techniques were chosen carefully.

ITO conductive substrates were used as the bottom substrates to create a smooth and conductive surface. Dion-Jacobson layered perovskite $Ca_2NaNb_3O_{10}$ (CNNO) nanosheets were used as the insulating material due to their high aspect ratio and can form compact and pores-free networks. To avoid the waste of the dispersion, dip coating was used and multi-layer deposition can be conducted using CNNO isopropanol dispersion. It is generally regarded that surface coverage can be improved with increasing coating numbers (film thicknesses). However, there are still small-sized pinholes existing on the film surface, especially if the layer is only tens of nanometers. These pinholes will develop metal filaments down to the bottom ITO if metal is sputtered on the top surface. To avoid this issue, we adopted high aspect ratio metallic nanosheets as the top electrode material, such as graphene and silver nanosheets. These nanomaterials could bridge the local pinholes and form intimate contact with CNNO to create uniform electrical field distribution. Spray coating was used to deposit metallic thin films through shadow masks to form patterns, so the device area can be defined by the overlapping area between the top and bottom electrodes. The morphological and electrical results will be presented in the corresponding deliverables

3.1.2 Fabrication of vertically stacked MSSSM devices

Light emitting diodes (LEDs) is a typical MSSSM device, that require carrier transport layers and light emissive layers sandwiched by two metal layers. They oftentimes rely on vertical structured devices where all layer thicknesses are around tens of to hundreds of nanometers to facilitate effective charge injection into the light emissive layer. The chosen material and its liquid should be able to spread evenly on the surface to form a thin film with a good surface morphology. A good spreading of dispersion normally requires the surface tension of the dispersion is lower than that of the substrate.[2] Moreover, each layer deposition should also guarantee the last deposited, underneath layer remains to be morphologically and electronically unaffected. In other words, a set of orthogonal solvents should be considered along with the functional materials.

Spin coating was chosen as the solution deposition method. This method will require a relatively high concentration of nanoparticles in liquids which is around tens of milligram per milliliter to maximise

surface coverage. The concentration of nanosheet dispersion was obtained by filtration and weighing a certain volume of dispersion.

We proposed a structure as ITO/PEDOT:PSS/poly-TPD/2DMs/ZnO/Al. In this structure, we attempted to use PEDOT:PSS as the hole injection layer and poly-TPD as the hole transport layer. Both are widely used polymeric transport layer materials. PEDOT:PSS was dispersed in an aqueous solution and is used on top of the transparent ITO electrodes on glass. To improve the PEDOT:PSS wettability on ITO surface, O_2 plasma was performed to ITO to increase the substrate surface tension. Poly-TPD is dissolved in chlorobenzene, which is a non-polar solvent that can work well with PEDOT:PSS without re-dispersing.[3] Therefore, CB based poly-TPD can be used on top of thermally annealed PEDOT:PSS.

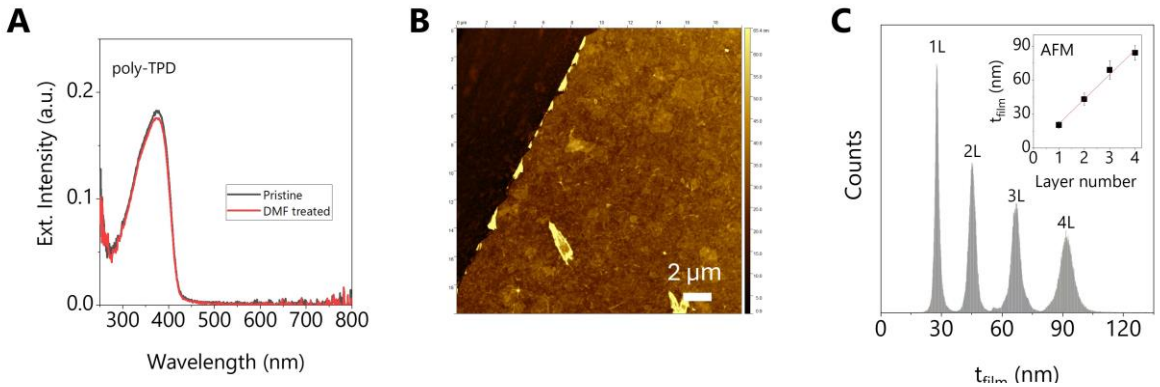

Figure 1 Characterisations of thin films. (A) Extinction spectra of poly-TPD film before and after DMF treatment, (B) A typical AFM image of a spin-coated MoS_2 nanosheet thin film, and (C) Histogram plots of thickness distribution of spin coated MoS_2 thin films with various thicknesses. The inset in (C) is the thicknesses extracted from AFM measurements against coating numbers. A linear fit is performed and the intercept is -0.04 nm, which confirms the good thickness scaling with coating numbers.

Next, we use electrochemically exfoliated MoS_2 as the model material owing to their high aspect ratio and mechanical flexibility. Such types of nanosheets can easily form compact thin films without open pores. We choose dimethylformamide (DMF) to disperse MoS_2 and deposit their thin films on poly-TPD. To verify, we spun coat DMF on poly-TPD and collected the extinction spectra before and after treatment (**Figure 1A**). The extinction peak at 375 nm is only reduced by less than 4%, meaning that the thickness changes is less than 4%. The extinction intensity at higher wavelengths remains around 0, which is a sign of no scattering component in the spectrum, confirming that DMF will not cause additional surface roughness.

MoS_2 DMF dispersion can be subsequently spun coated on poly-TPD. A typical AFM image of the spin coated MoS_2 thin film is shown in **Figure 1B**, that a compact layer is formed and nanosheets form conformal alignment. To tune the thickness of 2D network, spin coating can be repeated with a short annealing step before the next coating, e.g., 100 °C for 5 min. We prepared several samples on glasses with different coating numbers. Their optical transmission images were collected to extract the spatial variation information of the film thickness by converting the transmission into extinction intensity, which can be further correlated to the thickness measured by AFM. The detailed procedure is described in ref. [4]. The histogram plots of thickness were plotted against coating numbers (**Figure 1C**). For the thinnest film, the thickness distribution was not reaching to 0, implying that there was no large-sized pinholes on the film. Further, the thickness distribution for each coating number

shows minimum overlapping, meaning that each coating can build up thickness without re-dispersing the underneath film. The thicknesses measured by AFM are plotted against coating number as shown in **Figure 1C inset**, which shows the thickness scales reasonably linear, showing a minimum re-dispersing effect.

Next, ZnO nanoparticles in isopropanol were used as the electron transport layer materials. Isopropanol is a low surface tension solvent (23 mN m^{-1})[2] that exhibits optimum surface wettability on majority of commonly used substrates (20-50 mN m^{-1})[2], which is also suitable to be used on top of MoS_2 thin films. Importantly, the choice of ZnO nanoparticles could form seamless networks on top of 2D networks. During sputtering of the top electrode, e.g., aluminium Al, this network can prevent metal atoms from diffusing into 2D networks.

3.2 Contribution to project (linked) Objectives

The current deliverable will contribute to the following deliverables regarding morphological characterisations and devices. The fabrication protocols will be the foundation to realise other types of vertical heterostacked devices. In particular, we managed to realise first pinhole-free printed heterostack with all layer thickness <50 nm.

3.3 Contribution to major project exploitable result

4 Conclusion and Recommendation

To summarise, we identified the major fabrication issues for the solution-processed 2D vertical heterostacks as pinhole formation and re-dispersing. Several solution-processing techniques were used such as dip coating, spin coating, and spray coating. We chose high aspect-ratio insulating or semiconducting nanosheets to form compact and pores-free active layer. To decrease the pinhole density, multi-layer deposition of the identical material was realised by introducing a short annealing step before the next coating to densify the film and evaporate away the residual solvent. The formation of pinholes on the 2D layer can be therefore nearly eliminated. To avoid the ultra-small pinholes, we used high aspect ratio metallic nanosheets such as graphene or silver nanosheets to bridge over the pinholes and form an intimate electrical contact with the underneath layer. In another case, zero-dimensional nanoparticles can be used to form a compact layer on top of 2D layer to block the pinhole from forming conductive filament. The re-dispersing problem was overcome by a careful selection of orthogonal solvents throughout all the materials used in a heterostack.

Overall, we established the fabrication protocols for vertical heterostacks. It is expected that the proposed fabrication strategy can be further explored with many other types of material combinations and can be extended to various other types of devices.

5 Risks and interconnections

5.1 Risks/problems encountered

Risk No.	What is the risk	Probability of risk occurrence[1]	Effect of risk[1]	Solutions to overcome the risk

[1)] Probability risk will occur: 1 = high, 2 = medium, 3 = Low

5.2 Interconnections with other deliverables

The devices fabricated within D3.3 will be used for characterisation results covered in D4.1 about the characterisation on the heterostacks.

6 Deviations from Annex 1

No deviation.

7 References

[1] Gabbett, Cian, et al. "Quantitative analysis of printed nanostructured networks using high-resolution 3D FIB-SEM nanotomography." Nature Communications 15.1 (2024): 278.

[2] Hu, Guohua, et al. "Functional inks and printing of two-dimensional materials." *Chemical Society Reviews* 47.9 (2018): 3265-3300.

[3] Zhang, Shiming, et al. "Solvent-induced changes in PEDOT: PSS films for organic electrochemical transistors." *APL materials* 3.1 (2015).

[4] Cassidy, Oran, et al. "Layer-by-layer assembly yields thin graphene films with near theoretical conductivity." *npj 2D Materials and Applications* 9.1 (2025): 2.

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Project partners:

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1	TCD	TCD THE PROVOST, FELLOWS, FOUNDATION SCHOLARS & THE OTHER MEMBERS OF BOARD, OF THE COLLEGE OF THE HOLY & UNDIVIDED TRINITY OF QUEEN ELIZABETH NEAR DUBLIN
2	UNISTRA	UNIVERSITE DE STRASBOURG
3	UKa	UNIVERSITAET KASSEL
4	BED	BEDIMENSIONAL SPA
5	TUD	TECHNISCHE UNIVERSITAET DRESDEN
6	VSCHT	VYSOKA SKOLA CHEMICKO-TECHNOLOGICKA V PRAZE
7	UNR	UNIRESEARCH BV
8	UniBw M	UNIVERSITAET DER BUNDESWEHR MUENCHEN
9	EPFL	ECOLE POLYTECHNIQUE FEDERALE DE LAUSANNE

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9 Appendix A - Quality Assurance Review Form

The following questions should be answered by all reviewers (WP Leader, reviewer, Project Coordinator) as part of the Quality Assurance procedure. Questions answered with NO should be motivated. The deliverable author will update the draft based on the comments. When all reviewers have answered all questions with YES, only then can the Deliverable be submitted to the EC.

NOTE: This Quality Assurance form will be removed from Deliverables with dissemination level "Public" before publication.

Question	**WP Leader**	**Reviewer**	**Project Coordinator**
	Paolo Samori (UNISTRA)	Francesco Bonaccorso (BeD)	Jonathan Coleman (TCD)
1. *Do you accept this Deliverable as it is?*	Yes	Yes	Yes
2. *Is the Deliverable complete?* - *All required chapters?* - *Use of relevant templates?*	Yes	Yes	Yes
3. *Does the Deliverable correspond to the DoA?* - *All relevant actions preformed and reported?*	Yes	Yes	Yes
4. *Is the Deliverable in line with the 2D-PRINTABLE objectives?* - *WP objectives* - *Task Objectives*	Yes	Yes	Yes
5. *Is the technical quality sufficient?* - *Inputs and assumptions correct/clear?* - *Data, calculations, and motivations correct/clear?* - *Outputs and conclusions correct/clear?*	Yes	Yes	Yes
6. *Is created and potential IP identified and are protection measures in place?*	NA	NA	NA
7. *Is the Risk Procedure followed and reported?*	Yes	Yes	Yes
8. *Is the reporting quality sufficient?* - *Clear language* - *Clear argumentation* - *Consistency* - *Structure*	Yes	Yes	Yes

10 Appendix B - <<Appendix Title>>